Received 20 December 2017
Revised 18 June 2018
Accepted 6 July 2018

FCCSP IMC growth under reliability stress follows automotive criteria

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Abstract

Purpose – The Kirkendall void had been a well-known issue for long-term reliability of semiconductor interconnects; while even the KVs exist at the interfaces of Cu and Sn, it may still be able to pass the condition of unbias long-term reliability testing, especially for 2,000 cycles of temperature cycling test and 2,000 h of high temperature storage. A large number of KVs were observed after 200 cycles of temperature cycling test at the intermetallic Cu_3Sn layer which locate between the intermetallic Cu_6Sn_5 and Cu layers. These kinds of voids will grow proportional with the aging time at the initial stage. This paper aims to compare various IMC thickness as a function of stress test, the Cu_3Sn and Cu_6Sn_5 do affected seriously by heat, but Ni_3Sn_4 is not affected by heat or moisture.

Design/methodology/approach – The package is the design in the flip chip-chip scale package with bumping process and assembly. The package was put in reliability stress test that followed AEC-Q100 automotive criteria and recorded the IMC growing morphology.

Findings – The Cu_6Sn_5 intermetallic compound is the most sensitive to continuous heat which grows from 3 to 10 μm at high temperature storage 2,000 h testing, and the second is Cu_3Sn IMC. Cu_6Sn_5 IMC will convert to Cu_3Sn IMC at initial stage, and then Kirkendall void will be found at the interface of Cu and Cu_3Sn IMC, which has quality concerning issue if the void's density grows up. The first phase to form and grow into observable thickness for Ni and lead-free interface is Ni_3Sn_4 IMC, and the thickness has little relationship to the environmental stress, as no IMC thickness variation between TCT, uHAST and HTSL stress test. The more the Sn exists, the thicker Ni_3Sn_4 IMC will be derived from this experimental finding compare the Cu/Ni/SnAg cell and Ni/SnAg cell.

Research limitations/implications – The research found that FCCSP can pass automotive criteria that follow AEC-Q100, which give the confidence for upgrading the package type with higher efficiency and complexities of the pin design.

Practical implications – This result will impact to the future automotive package, how to choose the best package methodology and what is the way to do the package. The authors can understand the tolerance for the kind of flip chip package, and the bump structure is then applied for high-end technology.

Originality/value – The overall three kinds of bump structures, Cu/Ni/SnAg, Cu/SnAg and Ni/SnAg, were taken into consideration, and the IMC growing morphology had been recorded. Also, the IMC had changed during the environmental stress, and KV formation was reserved.

Keywords Automotive, IMC, Cu pillar, Kirkendall void, Solder bump

Paper type Research paper

The authors would like to thank ASE Group, Chung-Li QA lab team (Steven Shih) for supporting the reliability testing, and R&D lab team (Dr Fresh Tseng) for cross-section and SEM measurement.

PSU Research Review
Vol. 3 No. 1, 2019
pp. 70-83
Emerald Publishing Limited
2399-1747
DOI 10.1108/PRR-12-2017-0046

Abbreviation

KV = Kirkendall Void;
TCT = Temperature Cycling Test;
uHAST = unbias Humidity Accelerated Stress Test;
HTSL = High Temperature Storage Test;
IMC = Intermetallic Compound;
FCCSP = Flip Chip Chip Scale Package;
GPS = Global Position System;
RDL = Redistribution Layer;
JEDEC = Joint Electron Device Engineering Council;
DOE = Design of Experiment;
HAST = Humidity Accelerated Stress Test;
Min = Minimum;
FCLGA = Flip Chip Land Grid Array; and
RH = Relative Humidity.

1. Introduction

The automotive integrated circuit (IC) market will outgrow by two or even three times of the existing IC market. Market researchers predict that automotive semiconductors will occupy more than 15 per cent of the total semiconductor market by 2025, especially for those analog IC of intelligence vehicle. It is noteworthy that flip chip package becomes the automotive devices solution gradually because of the higher efficiency and complexities of the pin design. More and more design houses are moving toward flip chip or wafer-level fan-out package design for automotive infotainment, radar and GPS application. These changes will enable automobiles to become reliable and intelligent, so as let the packaging industry prioritize the development of advanced package for the next generation of automotive market requirements.

Focusing on the semiconductor industry, more and more devices turn their assembly form from legacy wire bonding to flip chip owing to the higher performance with shorter electrical signal transition path. Also, flip chip package can do more complex design, as the transition outset will not be limited at outer ring but full die area. wire bonding, the flip chip assembly requires the media-like pillar or solder bump to link signal between the chips and substrate; hence, the interconnection of the microstructural evolution do associate with effectiveness of reliability.

The Kirkendall void issue had been raised up (Wang *et al.*, 2009; Weinberg and Bohem, 2009; Tu, 2007), and lots of experts bring forward the view of why KVs were generated and how to inhibit the existing voids to extend the lifetime for electronic devices (Christine *et al.*, 2012; Liu *et al.*, 2013). The Kirkendall effect is the atomic movement of a diffusion system with the result of mass flow accompanying by a vacancy flow in the opposite direction. Although the voids exist at the intermetallic layer, the electrical signal may still be able to transit through the voids and passes the functional test. Adding Ni layer is the most common solution to extend the lifetime by blocking the Cu/Sn IMC diffusion, as it is more resistant to dissolution into solder joints (Lin *et al.*, 2008); yet, higher resistance will be because of the natural characteristic of Ni layer, and even some of the magnetic sensitive devices may have concern for adding these material; hence, the lifetime and void formation rate is extremely important for the device when to do the design from the initial stage.

2. Experimental works

The FCCSP daisy chain test vehicle applied for the current investigation was 6.64 × 4.98 mm die packaged in 9.60 × 9.60 mm with 211 I/O. The RDL daisy chain was designed not only at

substrate side but also at die side, so the open/short test could detect the entire signal net. The test vehicle's bonding diagram is shown in Figure 1.

The test vehicle was prepared following mainstream FCCSP manufacturing technology with four-layer die structure and three-layer ETS substrate; the schematic representation is shown in Figure 2. The die design is daisy chain RDL with two polyimide (PI) layers and plating bump, then flip chip onto substrate with mass reflow process. After molding, the substrate was singulated to single unit for open/short testing. Table I shows the configure uration of the package information of the daisy chain test vehicle structure.

3. Experimental plan

Three kinds of bump structure were selected and allocated with two passivation types which are well known as PI and polybenzoxazole (PBO). All the DOE legs are listed down in the Table II below.

Those DOE legs were built up with same mask, except for first layer of passivation, but just revised the mask tone for light transferred. The following daisy

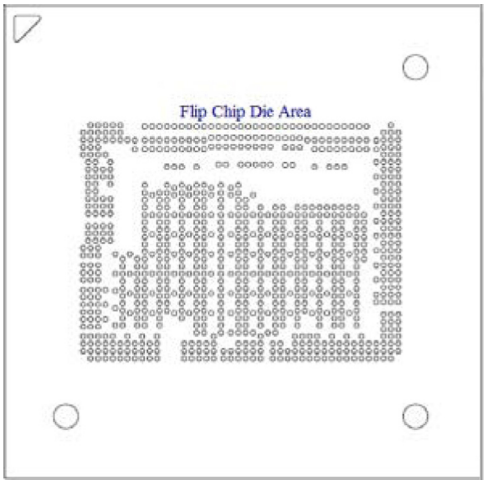


Figure 1.
FCCSP test vehicle bonding diagram

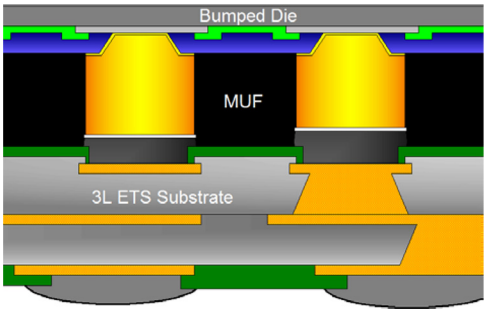


Figure 2.
Schematic of the FCCSP test vehicle

chain RDL and UBM process is the same. Hence, the three kinds of electrical connection point and passivation type were comparable for the automotive criteria reliability performance.

4. Testing procedures

The dies after grinding and sawing were assembled into daisy chained ETS test substrate which pad finish is bare Cu pads, and do molding process to protect the whole package. Then, the solder paste will be printed at substrate lead side. Before the long-term reliability testing, all the samples need to do final open short testing to ensure the signal is transmitted. Reliability testing was carried out according to JEDEC specifications and follow automotive AEC Grade 0 as shown in Table III shows.

The failure was judged by open short testing, and the failure criterion is zero failure from structure damage. In addition to the monitoring of IMC growing morphology, cross-section and scanning electron microscopy (SEM) to time zero and every reliability read point were performed.

Test vehicle feature	Description
Die side	
Structure	2 PSV with RDL and UBM
min pitch (μm)	150
RDL stackup	Ti/Cu/plated Cu
UBM stackup	Ti/Cu/plated Cu or Ni and SnAg
UBM diameter (um)	85
Substrate side	
Structure	FCLGA
Package size (mm)	9.6 × 9.6
Package thickness (mm)	775
min pitch (um)	500
Lead size (um)	260

Table I. Configuration of FCCSP TV

Leg	Passivation	Bump structure	Remarks
1	PI	Ni/SnAg	Standard solder bump
2		Cu/Ni/SnAg	Standard Cu pillar
3		Cu/SnAg	Ni-free pillar
4	PBO	Ni/SnAg	Plated solder bump with PBO
5		Cu/Ni/SnAg	Cu pillar with PBO
6		Cu/SnAg	Ni-free pillar with PBO

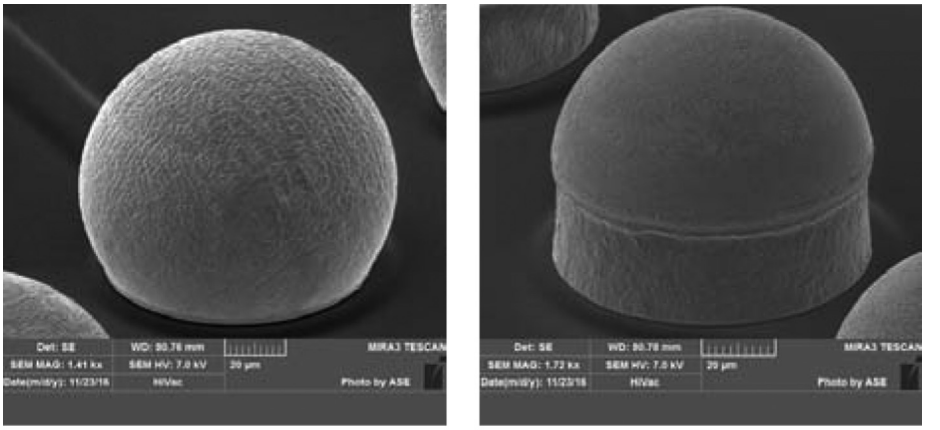
Table II. Design of experiment cell of PSV and bump structure

Reliability test item	Criteria (AEC Q100 Grade 0 Criteria)
Precondition JESD22-B112A	Level 3:30°C/60% RH 192 h
Unbias high temperature storage JESD-103	150°C, 500/1,000/1,500/2,000 h
Unbias HAST JESD22-A118	110°C/85% RH, 96/168/264hrs
Temperature cycling test JESD22-A104	−55-150°C, 500/1,000/1,500/2,000 cyc

Table III. Reliability testing criteria follow automotive AEC Q100 spec

5. Results and analysis

There are three kinds of bump structure such as Cu pillar with Ni barrier layer, Ni-free Cu pillar and plated solder bump, and the SEM of bumped structure is shown in Figure 3. The process flow is all the same but only different in plating sequence.



(a) (b)

Figure 3.
SEM of bumped die

Notes: (a) Plated solder bump; (b) plated Cu pillar

Leg	Passivation	Bump structure	Reliability test item	Test result
1	PI	Ni/SnAg	Precondition Lv3	0/77
2			Precon + uHAST 96/168/264 h	0/77
3			Precon + TCT 500/1,000/1,500/2,000 cyc	0/77
4			HTSL 500/1,000/1,500/2,000 h	0/77
5		Cu/Ni/SnAg	Precondition Lv3	0/77
6			Precon + uHAST 96/168/264 h	0/77
7			Precon + TCT 500/1,000/1,500/2,000 cyc	0/77
8			HTSL 500/1,000/1,500/2,000 h	0/77
9		Cu/SnAg	Precondition Lv3	0/77
10			Precon + uHAST 96/168/264 h	0/77
11			Precon + TCT 500/1,000/1,500/2,000 cyc	0/77
12			HTSL 500/1,000/1,500/2,000 h	0/77
13	PBO	Ni/SnAg	Precondition Lv3	0/77
14			Precon + uHAST 96/168/264 h	0/77
15			Precon + TCT 500/1,000/1,500/2,000 cyc	0/77
16			HTSL 500/1,000/1,500/2,000 h	0/77
17		Cu/Ni/SnAg	Precondition Lv3	0/77
18			Precon + uHAST 96/168/264 h	0/77
19			Precon + TCT 500/1,000/1,500/2,000 cyc	0/77
20			HTSL 500/1,000/1,500/2,000 h	0/77
21		Cu/SnAg	Precondition Lv3	0/77
22			Precon + uHAST 96/168/264 h	0/77
23			Precon + TCT 500/1,000/1,500/2,000 cyc	0/77
24			HTSL 500/1,000/1,500/2,000 h	0/77

Table IV.
Reliability testing matrix table

After bumping process, the three kinds of structure are packaged onto three-layer substrate with same process flow. The open/short can sort out functional pass units and then send for long-term reliability testing.

The long-term reliability testing results are summarized in Table IV. All the DOE legs pass automotive reliability criteria followed by AEC Q100 Grade 0 condition. Each condition had released 77 units for testing, and does open/short testing after each read point, and no failure was found when finishing overall conditions. Besides, one sample of each read point was picked up for the cross-section to study the IMC growing morphology.

The IMC growing thickness and analysis are summarized as following. T0 represents the bumped die joint to substrate with one time reflow only, and the sections for Ni-free pillar, Cu pillar and solder bump are shown in Figure 4. The IMC thickness at the interface of pillar Cu and solder, Ni and solder is monitored and recognized because of the KV that will be found at the Ni-free pillar condition and then compared to Ni barrier layer cell.

Among all of the DOE conditions, no recognized key factor related to passivation type, the possible reason is that those dies were protected in the molding under-fill, hence the passivation type not impact to the result, so as only the bump structure and read point are comparable.

IMC layer thickness of time zero and final read point 2,000 temperature cycles are shown in Figure 5. There are two kinds of IMC at the interface of Cu and Pb-free solder of Ni-free pillar cell, due to the atomic inter-diffusion, Cu_6Sn_5 IMC will be formed at the interface of Cu and solder, then Cu_3Sn layer grows accompany with thermal stress. Ni_3Sn_4 is the IMC

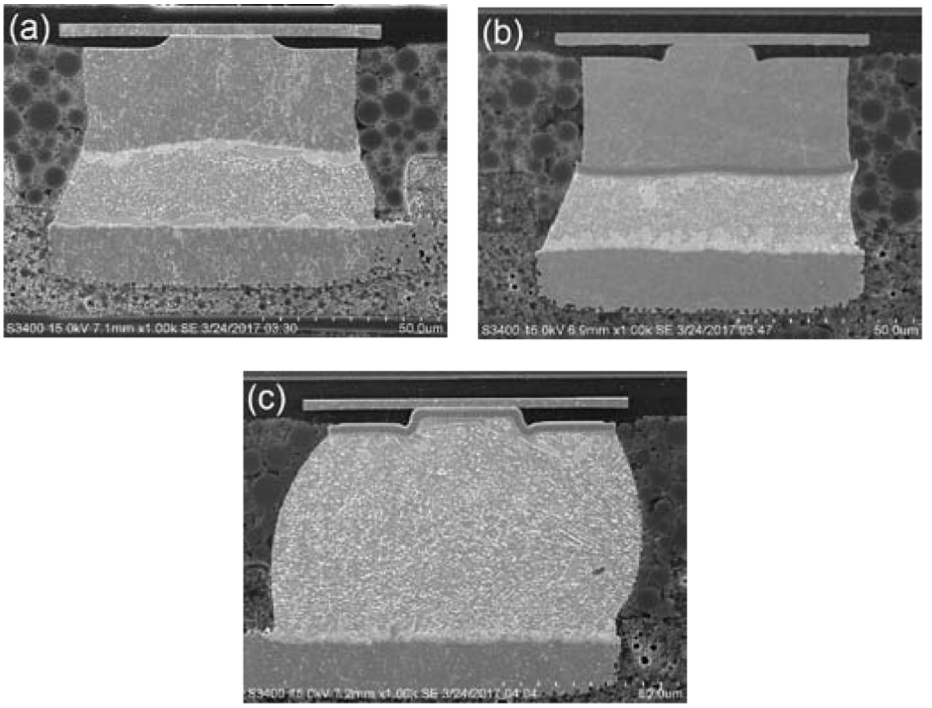


Figure 4.
Cross-section of T0

Notes: (a) Ni-free pillar; (b) Cu pillar; (c) solder bump

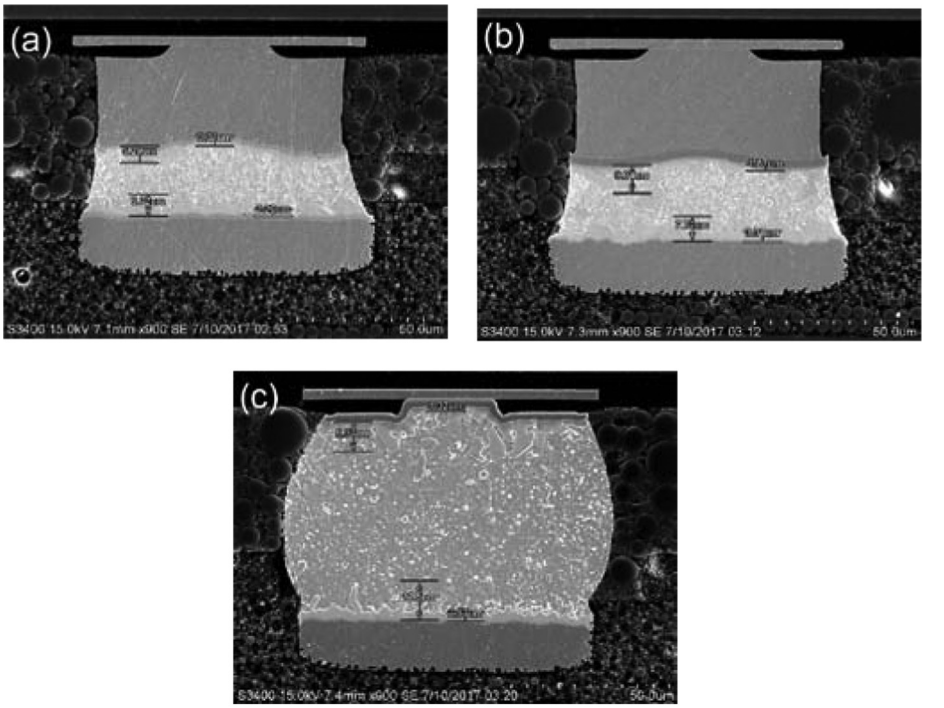


Figure 5.
Cross-section of TCT 2,000 cycles

Notes: (a) Ni-free pillar; (b) Cu pillar; (c) solder bump

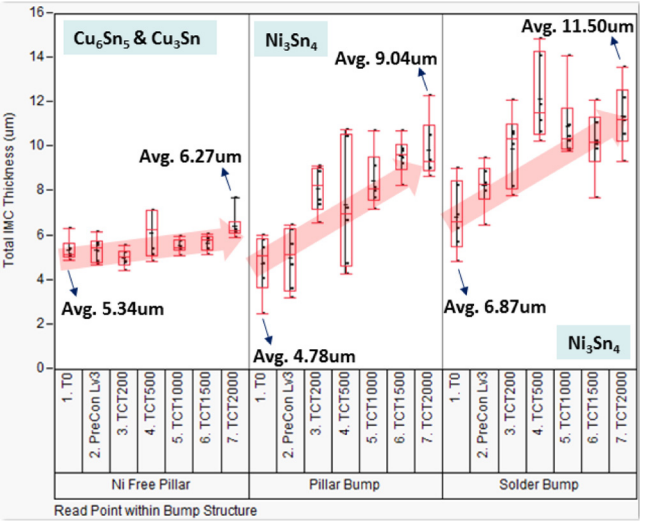


Figure 6.
IMC growing thickness under TCT stress test

formation of the Ni and Pb-free solder, which can be found at the Cu pillar and solder bump cell. Ni_3Sn_4 is the first phase to form and grow into observable thickness in a solid Ni/liquid Sn reaction couple during process.

Precondition and temperature cycling test of the IMC growing morphology is shown in Figure 6. The IMCs are growing steadily with thermal stress. From the chart, it is obviously that the Cu_6Sn_5 and Cu_3Sn growing rates are different from Ni_3Sn_4 IMC with lower growing rate.

If separate, the Cu_6Sn_5 and Cu_3Sn IMC thickness for the analysis is shown in Figure 7, and it can be found that the Cu_6Sn_5 IMC thickness has slightly decreased, and then grows when the thermal stress has increased. Furthermore, the Cu_3Sn IMC thickness has an increasing rate from time zero to precondition but cease to grow up when the temperature

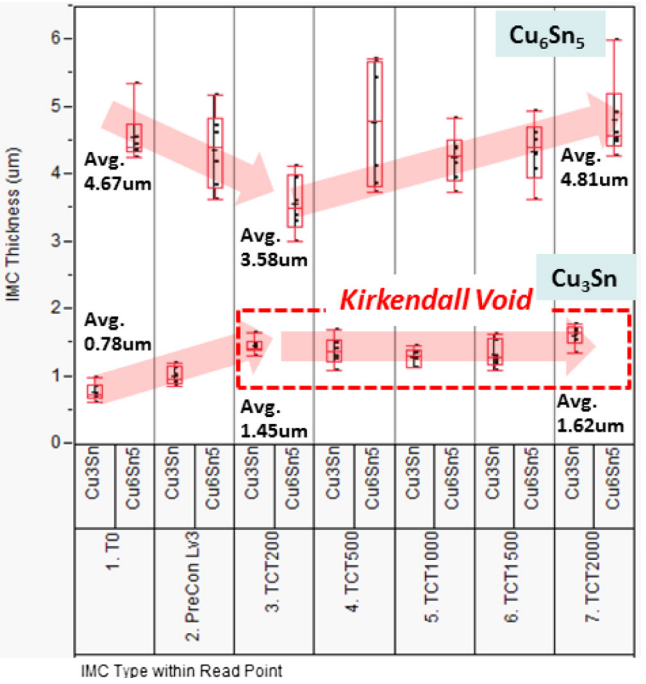


Figure 7.
Cu_6Sn_5 and Cu_3Sn IMC thickness under TCT stress test

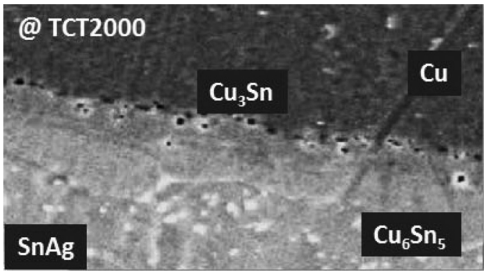


Figure 8.
Zoom in section for Ni-free pillar at TCT 2,000 cycles

cycling stress join, but the quality concerned with Kirkendall void was found from 200 cycles at Cu_3Sn IMC layer as shown in Figure 8.

The IMC thickness under unbias HAST test result is shown in Figure 9. It is under same phenomenon as temperature cycling stress, Ni_3Sn_4 grows fast accompany with the

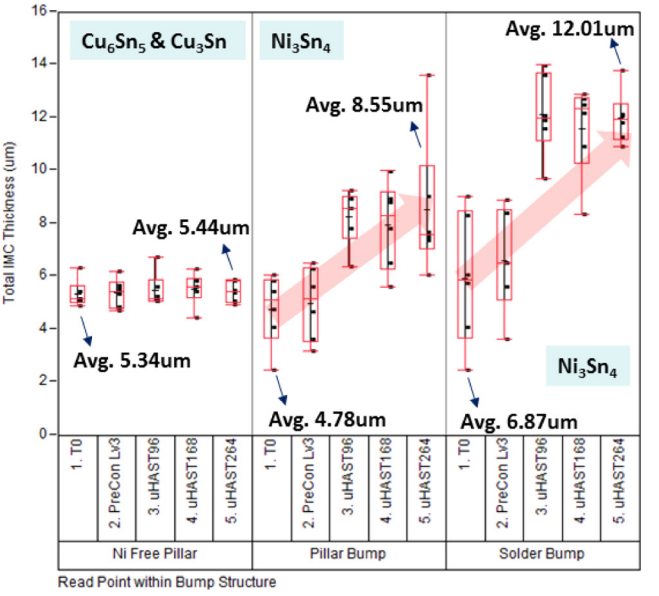


Figure 9.
IMC growing thickness under uHAST stress test

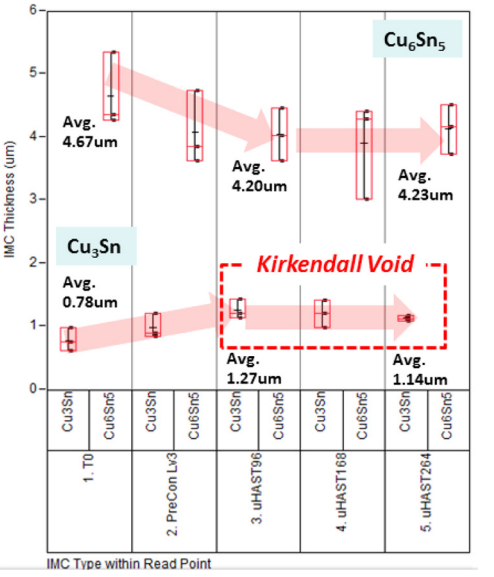


Figure 10.
Cu_6Sn_5 and Cu_3Sn IMC thickness under uHAST stress test

thermal stress, but Cu_6Sn_5 and Cu_3Sn IMC thickness not showing much difference. The Figure 10 shows Cu_6Sn_5 and Cu_3Sn IMC thickness separately, and Cu_6Sn_5 IMC also covert to Cu_3Sn IMC when the environmental stress participate in, then keep in steady even the testing hours from 96 to 264. The 110°C is not affected to the IMC growing morphology in evidence, but the atomic interdiffusion still exists. The KV issue as Figure 11 under uHAST test is not as serious as temperature cycling test, as the added stress is less in temperature and time.

The last test condition need to be discussed is high temperature storage which is the most rigorous to IC testing. From the IMC growing thickness analysis in Figure 12, the Cu_6Sn_5 and Cu_3Sn IMC grow faster than Ni_3Sn_4 IMC, at 2,000 read point, and the total thickness exceed 12 μm which may be the half of the solder standoff height. The environmental 150°C does affect the Cu-Sn IMC growing morphology but does not affect the Ni-Sn IMC layer, which remains the same growing rate as per the previous two conditions.

The Figure 13 explains the Cu_6Sn_5 IMC thickness that will be influenced by the continuous heat stress, and part of the Cu_6Sn_5 IMC converts to Cu_3Sn IMC, and then itself grows up accompanying with the stress time and grows up to near average 10 μm. The

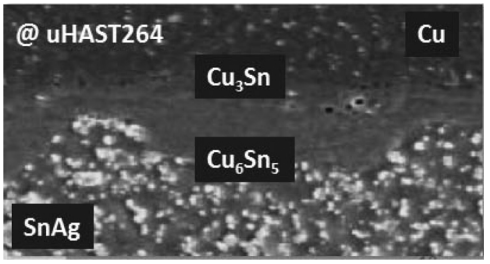


Figure 11.
Zoom in section for Ni-free pillar at uHAST 264 h

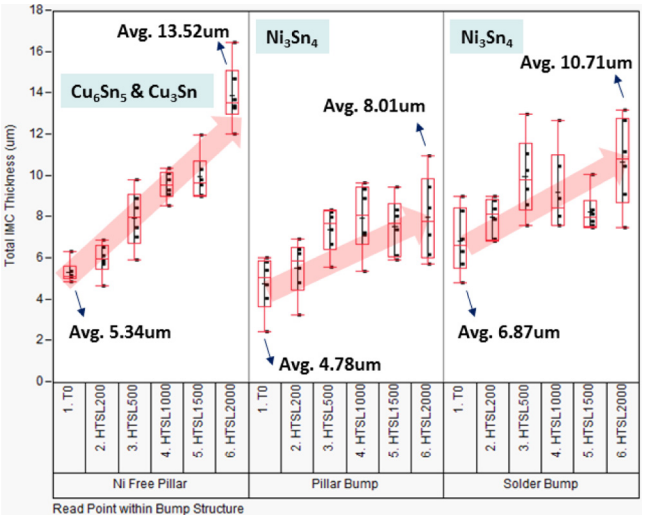


Figure 12.
IMC growing thickness under HTSL stress test

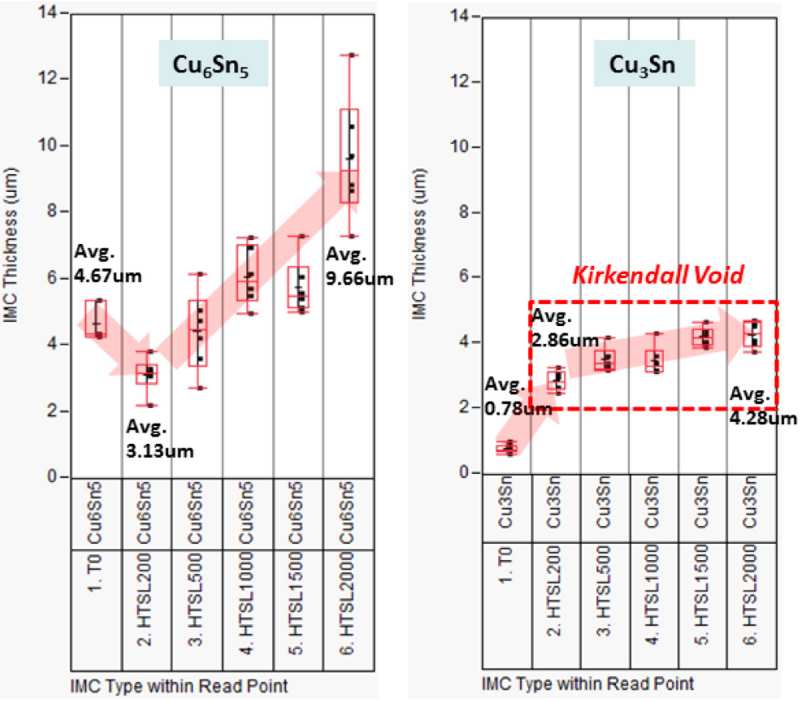


Figure 13.
Cu_6Sn_5 and Cu_3Sn IMC thickness under HTSL stress test

Cu_3Sn IMC also be impacted by the heat stress slightly, it did not keep the layer thickness, but become thicker with the time under heating. Also, the KV quality is critical for those voids that almost connect to each other as Figure 14 shows up. Yet, even under this full of void situation, the open/short testing still gives green light for the electrical signal transition pass.

When Cu contact with liquid Sn under the temperature range of 112-227°C, the diffusivity of Cu in Sn was much faster, and the intermetallic compounds will be formed in the interphase region which can be derived from the binary Cu-Sn phase diagram as in Figure 15. The intermetallic $Cu_6Sn_5(\eta)$ is important because of the large number of tin–lead and lead-free solder joints formed directly to copper. This IMC forms an interfacial layer and can be found in the bulk microstructure solder joints where

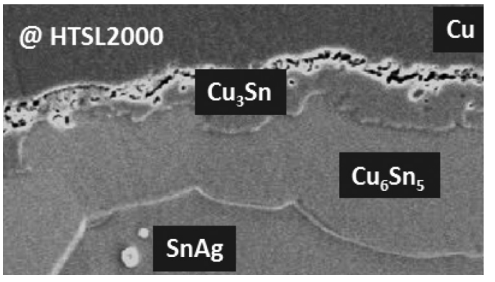
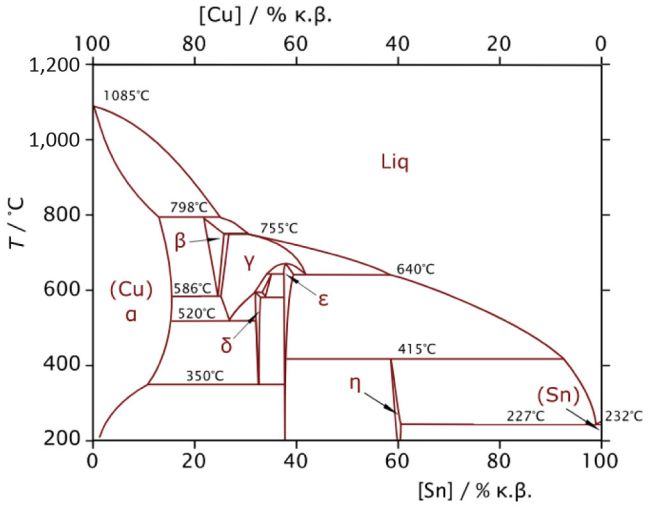


Figure 14.
Zoom in section for Ni-free pillar at HTSL 2,000 hrs



Source: Massalski (1996)

Figure 15.
Binary Cu-Sn phase diagram

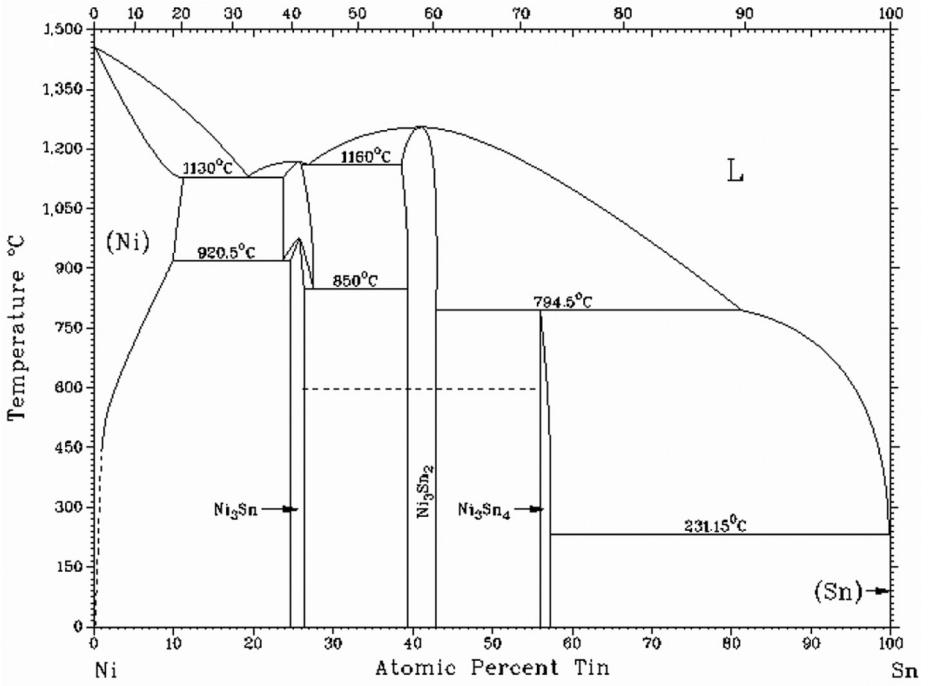


Figure 16.
Binary Ni-Sn phase diagram

excessive time and temperature are involved during the soldering process, and Cu_3Sn (ε) will be converted and grown. The formation of the ε phase and the interrelationship between the ε phase and the η phase growth are more complicated (Tu, 1973; Tu and Thompson, 1982; Clevenger *et al.*, 1998). However, the $Cu_3Sn(\varepsilon)$ is the IMC that unwilling to be found since the KV usually located in this layer.

The growth kinetics of the Ni_3Sn_4 phase appeared to be parabolic and diffusion-controlled (Oh, 1994). Ni_3Sn_4 IMC is the first phase to form and grow into observable thickness in a solid Ni/liquid Sn reaction couple which will be derived from the Ni-Sn binary diagrams as shown in Figure 16. After the formation of continuous Ni_3Sn_4, further growth occurs as a result of the diffusion of Sn through the intermetallic layer. The other three equilibriums Ni IMCs, Ni_3Sn_2 and Ni_3Sn grow with much slower kinetics and have difficulties in nucleating at the Ni/Sn interface. In both Ni_3Sn_2 and Ni_3Sn, the main diffusing species during the growth is Ni (Bader *et al.*, 1995).

6. Conclusions

- The FCCSP package can pass through automotive reliability criteria that follow AEC Q100 Grade 0 condition, with solder bump or Cu pillar structure, and the molding underfill only can protect fragile dies from the environmental stress.
- The Cu_6Sn_5 intermetallic compound is the most sensitive to continuous heat which grows from 3 to 10 μm at high temperature storage 2,000 h testing, and the second is Cu_3Sn IMC.
- Cu_6Sn_5 IMC will convert to Cu_3Sn IMC at the initial stage, and then Kirkendall void will be found at the interface of Cu and Cu_3Sn IMC, which has the quality concerning issue if the void's density grows up.
- The first phase to form and grow into observable thickness for Ni and lead-free interface is Ni_3Sn_4 IMC, and the thickness has little relationship to the environmental stress, as no IMC thickness variation between TCT, uHAST and HTSL stress test.
- The more the Sn exists, the thicker Ni_3Sn_4 IMC will be derived from this experimental finding compare the Cu/Ni/SnAg cell and Ni/SnAg cell.

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